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Methods Of Forming Conductive Capacitor Plugs, Methods Of Forming Capacitor Contact Openings, And Methods Of Forming Memory Arrays

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METHODS OF FORMING CONDUCTIVE CAPACITOR PLUGS, METHODS OF FORMING CAPACITOR CONTACT OPENINGS, AND METHODS OF FORMING MEMORY ARRAYS

TECHNICAL FIELD

This invention relates to methods of forming conductive capacitor plugs, to methods of forming capacitor contact openings, and to methods of forming memory arrays.

BACKGROUND OF THE INVENTION

Semiconductor processing involves a number of processing steps in which individual layers are masked and etched to form semiconductor components. Mask alignment is important as even small misalignments can cause device failure. For certain photomasking steps, proper alignment is extremely critical to achieve proper fabrication. In others, design rules are more relaxed allowing for a larger margin for alignment errors. One way in which design rules can be relaxed is to provide processing sequences which enable so-called self aligned etches, such as to encapsulated word lines in the fabrication of memory circuitry. Further, there is a goal to reduce or minimize the number of steps in a particular processing flow. Minimizing the processing steps reduces the risk of a processing error affecting the finished device, and reduces cost.

This invention arose out of needs associated with improving the manner in which semiconductor memory arrays, and in particular capacitor-over-bit line memory arrays, are fabricated.

SUMMARY OF THE INVENTION

Methods of forming conductive capacitor plugs, methods of forming capacitor contact openings, and methods of forming memory arrays are described. In one embodiment, a conductive capacitor plug is formed to extend from proximate a substrate node location to a location elevationally above all conductive material of an adjacent bit line. In another embodiment, a capacitor contact opening is etched through a first insulative material received over a bit line and a word line substantially selective relative to a second insulative material covering portions of the bit line and the word line. The opening is etched to a substrate location proximate the word line in a self-aligning manner relative to both the bit line and the word line. In another embodiment, capacitor contact openings are formed to elevationally below the bit lines after the bit lines are formed. In a preferred embodiment, capacitor-over-bit line memory arrays are formed.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a top plan view of the semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a different processing step.

Fig. 3 is a view which is taken along line 3-3 in Fig. 2.

Fig. 4 is a view of the Fig. 3 wafer fragment at a different processing step.

Fig. 5 is a view of the Fig. 4 wafer fragment at a different processing step.

Fig. 6 is a view of the Fig. 5 wafer fragment at a different processing step.

Fig. 7 is a view of the Fig. 6 wafer fragment at a different processing step.

Fig. 8 is a view of the Fig. 2 wafer fragment at a different processing step.

Fig. 9 is a view which is taken along line 9-9 in Fig. 8.

Fig. 10 is a view of the Fig. 9 wafer fragment at a different processing step.

Fig. 11 is a view of the Fig. 10 wafer fragment at a different processing step.

Fig. 12 is a view of the Fig. 11 wafer fragment at a different processing step.

Fig. 13 is a view of the Fig. 12 wafer fragment at a different processing step.

Fig. 14 is a view which is taken along line 14-14 in Fig. 8 and somewhat reduced in dimension.

Fig. 15 is a view of the Fig. 14 wafer fragment at a different processing step.

Fig. 16 is a view of the Fig. 15 wafer fragment at a different processing step.

Fig. 17 is a view of a semiconductor wafer fragment in process, in accordance with another embodiment of the invention. The Fig. 17 view coincides to processing which can occur after the view depicted in Fig. 12.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment 20 in process in accordance with one embodiment of the invention includes a semiconductive substrate 22. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other

materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Substrate 22 includes a plurality of active areas 24 and a plurality of isolation regions 26. Isolation regions 26 can be formed through various techniques including shallow trench isolation.

Referring to Figs. 2 and 3, a plurality of conductive lines 28 are formed over substrate 22 and constitute word lines of a memory array which is to be formed. Each of word lines 28 includes a gate oxide layer 30, a conductive polysilicon layer 32, and an overlying silicide layer 34. Insulative coverings are formed over individual word lines 28 and include sidewall spacers 36 and an insulative cap 38. The insulative coverings preferably encapsulate the word lines. Exemplary insulative materials include oxide formed through decomposition of TEOS, or nitride/oxynitride materials. Diffusion regions 40 are provided and formed intermediate word lines 28 and define substrate node locations with which electrical communication is desired. The illustrated diffusion regions include lightly doped drain (LDD) regions (not specifically designated).

Referring to Fig. 4, a first layer 42 is formed over substrate 22 and between conductive lines 28 and comprises a first insulative material which is different from the insulative material covering or encapsulating word lines 28. An exemplary material is borophosphosilicate glass (BPSG) which can be subsequently reflowed and planarized as by conventional techniques to provide a generally planar uppermost

surface 44. A first masking layer 46 is formed over the substrate and defines a plurality of bit line plug mask openings 48. An exemplary material is photoresist.

Referring to Fig. 5, material of first layer 42 is etched through bit line plug mask openings 48 and individual substrate diffusion regions 40 between selected word lines 28 are preferably exposed. Such etching forms bit plug openings 50 intermediate the selected word lines.

Referring to Fig. 6, conductive material 52 is formed over and in electrical communication with the individual substrate diffusion regions 40 beneath bit plug openings 50 (Fig. 5). An exemplary material is conductively doped polysilicon which can be deposited, and portions subsequently removed, to isolate the conductive material within the bit plug openings and form individual plugs 54. Plugs 54 can be formed by chemical mechanical polishing conductive material 52 or through various etch back techniques.

Referring to Figs. 7 and 8, individual bit lines 56 are formed and in electrical communication with respective individual conductive bit line plugs 54. Bit lines 56 are formed over insulative material 42 and the illustrated word lines 28. Bit lines 56 include a polysilicon layer 58 and a silicide or other conductive layer 60 (i.e., tungsten). An insulative covering 62 is formed over conductive material of the bit lines and can comprise a suitable oxide, such as one formed through decomposition of TEOS, or nitride/oxynitride materials. The various bit line layers are preferably blanket deposited over the substrate and

subsequently photomasked and etched to provide the illustrated bit lines (Fig. 8). Alternately, the bit line plug and the bit line can comprise a common material deposited during the same processing step. For example, layers 52 and 58 could comprise the same material which is deposited thick enough to form both the conductive plug and some or all of bit lines 56.

Referring to Fig. 9, a view is shown which is taken along line 9-9 in Fig. 8 and cuts across three individual bit line plugs 54 and their associated bit lines 56.

Referring to Fig. 10, a layer of insulative material is formed over substrate 22 and etched to provide insulative coverings in the form of sidewall spacers 64. Sidewall spacers 64 together with insulative coverings 62 serve to encapsulate the individual bit lines. It will be appreciated, however, that the insulative material which ultimately becomes sidewall spacers 64 need not be etched to form the sidewall spacers at this time. Exemplary materials for insulative material 64 include oxide formed through decomposition of TEOS, or nitride/oxynitride materials. In a preferred embodiment, the insulative material which is utilized to encapsulate the word lines (Fig. 3) is the same material which is utilized to encapsulate the bit lines.

Referring to Fig. 11, a second layer 66 is formed over the word lines and bit lines 56, and preferably comprises the first insulative material which was formed over word lines 28, e.g. BPSG. Such layer is preferably reflowed and planarized. Layers 42, 66 constitute a

plurality of separately-formed layers of first insulative material which, in the preferred embodiment, comprise two layers.

Referring to Fig. 12, a second patterned masking layer 68 is formed over second layer 66 and defines a plurality of opening patterns 70 over various substrate diffusion regions 40. Openings 70 are formed on opposite sides of individual word lines between which individual bit line plugs are formed. A preferred alternative to forming individual openings 70 over the illustrated diffusion regions is to form a so-called stripe opening which can be opened up over a plurality of the diffusion regions, where of the stripe opening intersects with the bit line spaces. An exemplary stripe opening is illustrated in Fig. 8 inside dashed line 72 (Fig. 8).

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Whether individual openings 70 are formed in second masking layer 68 or stripe opening 72 is formed, capacitor contact openings 74 are etched through first and second layers of insulative material 42, 66 respectively. In the illustrated example, capacitor contact openings 74 are etched to elevationally below bit lines 56, down to proximate individual word lines of the memory array. In a preferred embodiment, the etching exposes individual diffusion regions 40. In this example, and because individual openings 70 are formed in second masking layer 68, some portions of second layer 66 remain over the individual bit lines. Where, however, the above-mentioned stripe opening 72 (Fig. 8) is formed, all of first insulative material 66 over the individual bit lines would ideally be removed.

In a preferred embodiment, the material which is used to encapsulate both the bit lines and the word lines is selected to comprise the same material, or, a material selective to which layers 42, 66 can be etched. Accordingly, etch chemistries can be selected to etch material of both layers 42, 66 substantially selectively relative to the material encapsulating both the word lines and the bit lines. Hence, capacitor contact openings 74 can be formed in a self-aligning manner to be generally self-aligned to both the bit lines and the word lines. Aspects of the invention also include non-capacitor-over-bit line memory array fabrication processes, and selective etching of contact openings which might not be capacitor contact openings.

Referring to Figs. 13 and 14, conductive material 76 is formed within individual contact openings 74 and in electrical communication with individual respective diffusion regions 40. An exemplary material is conductively doped polysilicon which can be subsequently etched back or chemical mechanical polished to form individual capacitor plugs 78. In the illustrated example, conductive material 76 extends from proximate diffusion regions 40 to respective elevations which are at least laterally proximate (including higher) individual conductive portions of the bit lines. In a preferred embodiment, conductive material 76 extends to locations which are elevationally higher than any conductive portion of any bit line. Individual conductive capacitor plugs 78 include

individual surfaces 80 proximate which each plug terminates. Surfaces 80 are disposed at elevations above conductive portions of the bit lines.

Referring to Figs. 15 and 16, an insulative layer 82, e.g. BPSG, is formed over the substrate and subsequently patterned and etched to form individual capacitor containers 84 (Fig. 16). Storage capacitors are then formed by depositing a storage node layer 86, a cell dielectric layer 88, and a cell plate layer 90. Accordingly, such constitutes a portion of a capacitor-over-bit line memory array.

In but one aspect, the above methods can facilitate formation of memory circuitry over other techniques wherein the capacitor plugs are formed prior to formation of the bit lines. Such other techniques can present alignment problems insofar capacitor container-to-bit line, and capacitor container-to-word line, alignments are concerned. Aspects of the present invention can permit the capacitor plugs to be formed to be generally self-aligned to both the word lines and the bit lines, while preserving the mask count necessary to form the subject memory arrays. Other aspects of the present invention can ease alignment constraints imposed on capacitor container alignment by removing requirements that the containers be etched to be self-aligned to other structures including the bit lines.

Referring to Fig. 17, and in accordance with an alternate embodiment of the present invention, storage capacitors can be formed directly within contact openings 74 (see Fig. 12) such that capacitor plugs 78 (Fig. 13) are not necessary. Like numbers from the above-

described embodiment have been utilized where appropriate, with differences being indicated with the suffix "a". A layer 66a is formed over the substrate and subsequently patterned and etched, along with layer 42 as described above, to form capacitor containers 84a. Subsequently, storage capacitors are formed by depositing a storage node layer 86a, a cell dielectric layer 88a, and a cell plate layer 90a. Accordingly, such constitutes forming conductive material at least partially within individual contact openings 74. The above storage capacitor constructions are for illustrative purposes only. Accordingly, other constructions are possible. For example, and by way of example only, plugging material 76 of Figs. 13 and 14 might be etched partially inward to provide more room, and thereby more capacitance, for the capacitor being formed. Further and by way of example only, some or all of the insulative material laterally outside of the capacitor container might be etched away in advance of forming the capacitor dielectric layer to provide more surface area and thereby more capacitance. Memory cells of the invention can be fabricated to occupy $6F^2$, $8F^2$ or other areas, with $6F^2$ being preferred.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or

modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.